Thermal head printer 128 Bit driver (Gold Bumped)

March 2018

GENERAL DESCRIPTION

The FS9010 is a 128-bit CMOS driver designed for the thermal printer head. The driver include 128 built-in shift registers to transfer the data, and 128 latches to hold the input data. In general, “H” or “L” levels can be selected for the latch and strobe control.

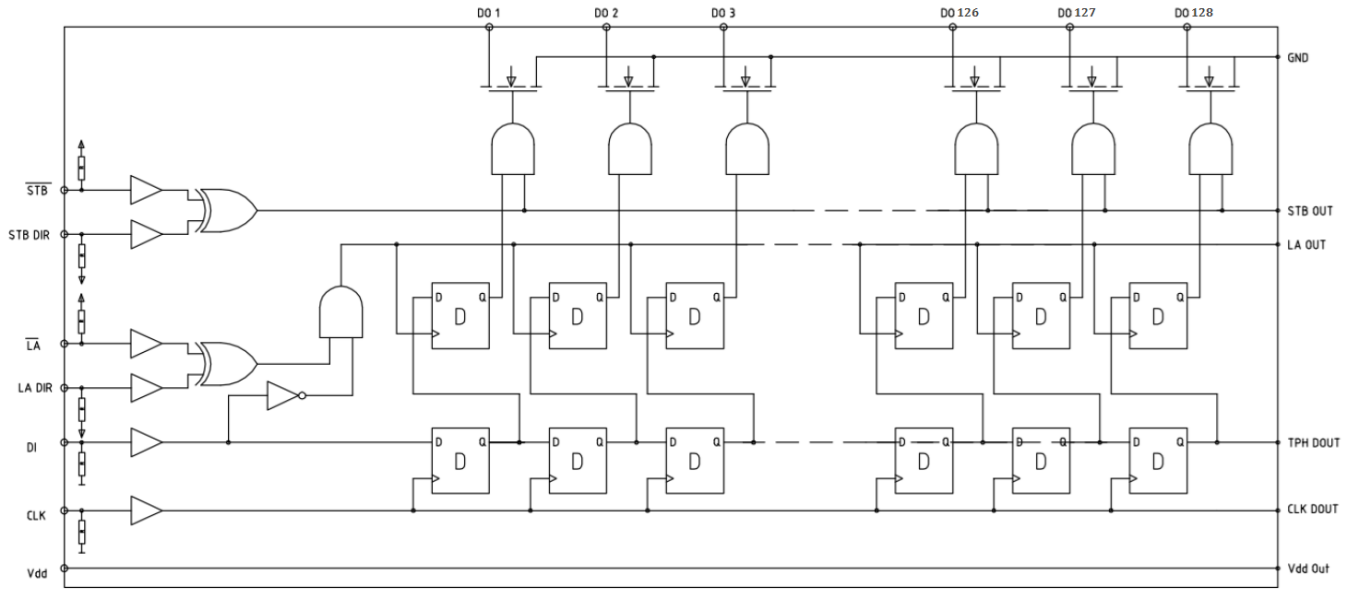
FEATURES

- Low current consumption: 1mA typ (VDD=3.3V, Fclk 6Mhz, Din fixed low)
- High speed operation: 16 Mhz (daisy chain)
- Driver off function when supply voltage drops
- Driver output max voltage: up to 40 v
- Ron (open drain saturated resistance): 12Ω

APPLICATIONS

- Thermal printer head

FUNCTIONAL BLOCK DIAGRAM



Operation Description

The 128-bit shift register reads the data from input, DI, on the rising edge of the CLK. The operation of 128-bit latches depends on the logic level of LAT. The latches reads the data from shift register when LAT level is low, and it holds the data of the shift register when LAT is different. The data in 128-bit latches controls the respective output high-voltage drivers when STB is low and STB_DIR is high. The driver high-voltage output transistor turns on if the corresponding latch data is high, and off if low. Setting STB high or STB_DIR low disables all driver output transistors. The operation and relationship of these control signals are shown as below:

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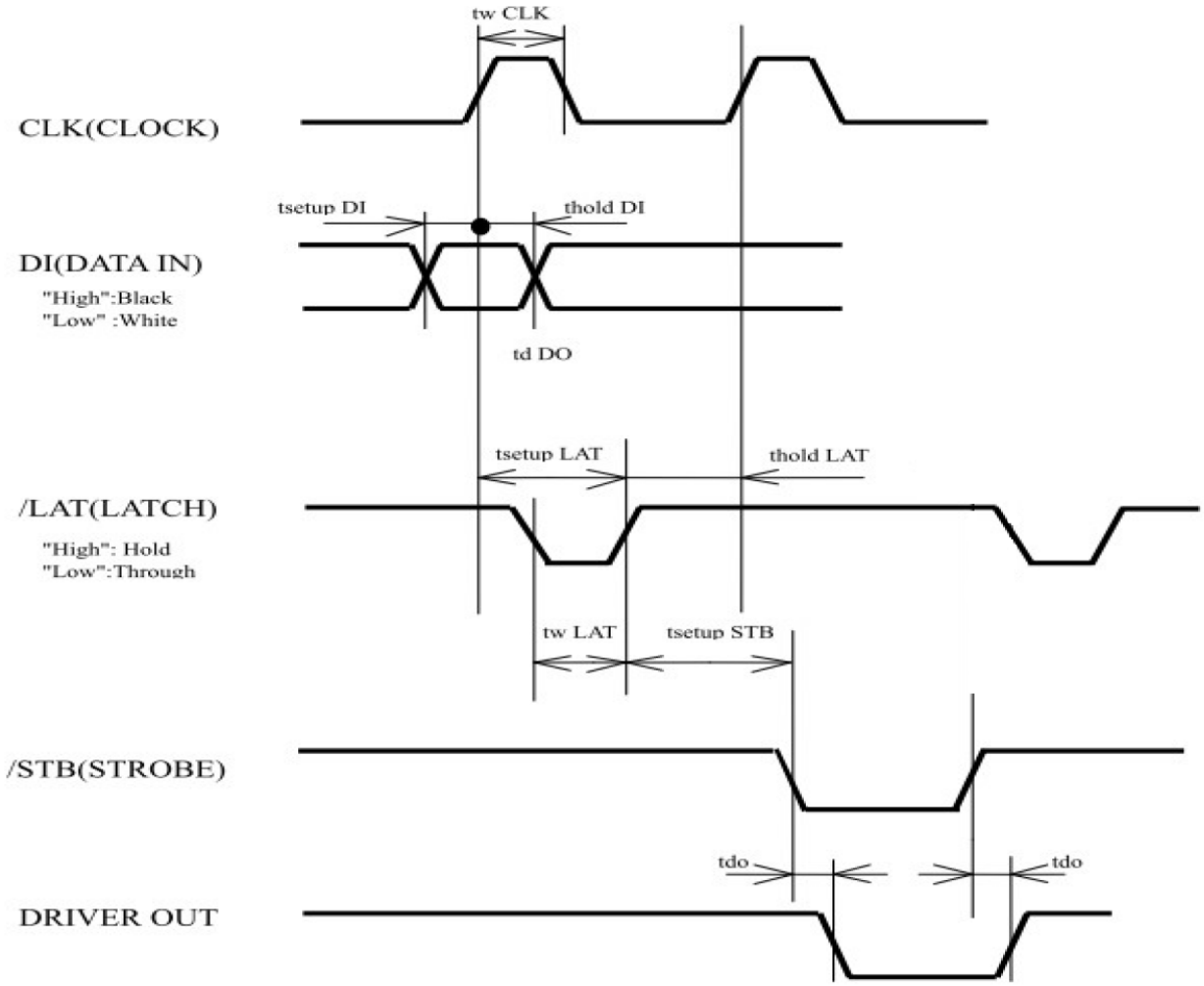

Pin Information

PAD Name	I/O	Description
DI	I	Serial data input terminal for 128-bit shift register
TPH_DOUT	O	Serial data output terminal for 128-bit shift register
CLK	I	Clock input terminal
CLK_OUT	O	Clock output terminal
LAT_B	I	Data latch signal control terminal : a. When LAT_DIR="H" & LAT_B="H" : holds the preceding data When LAT_DIR="H" & LAT_B="L" : reads the data of the shift register b. When LAT_DIR="L" & LAT_B="L" : holds the preceding data When LAT_DIR="L" & LAT_B="H" : reads the data of the shift register c. LAT_B : pull-up resistor is built-in. LAT_DIR: pull-down resistor is built-in.
LAT_DIR	I	
LAT_OUT	O	Latch output terminal
STB_B	I	Data enable signal control terminal : a. When STB_DIR="H" &STB_B="H" : disable the output When STB_DIR="H" & STB_B="L" : outputs the latch data to driver b. When STB_DIR="L" &STB_B="L" : disable the output When STB_DIR="L" &STB_B="H" : outputs the latch data to driver c. STB_B : pull-up resistor is built-in. STB_DIR: pull-down resistor is built-in.
STB_DIR	I	
STB_OUT	O	STB output terminal
VDD		Positive power supply for logic function (2.7V~5.5V)
GND		Ground for logic function and driver
DO1-DO128	O	Driver output terminals (open-drain NMOS)

ABSOLUTE MAXIMUM RATINGS

Do1,Do2…Do128 to GND Voltage	-0.3V ~ 45V
STB_B, STB_DIR, LA_B, LA_DIR, DI, CLK, vdd, vdd_out, STB_OUT, LA_OUT, TPH_OUT, CLK_OUT to GND Voltage	-0.3V ~ 6V
Operation frequency	4 MHz
Operating temperature range, T_A	-40°C~85°C
Storage temperature range, T_{STG}	-55°~+150°C
ESD (HBM)	2000 V
Latch-up	+/- 100mA

Note:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test condition is T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified.

Item	Symbol	Min.	Typ.	Max.	Unit
Voltage at open Drain	VH			40	V
Logic voltage	VDD	2.7	3.3	5.5	V
Max open Drain saturated Resistance	Ron		12		Ohms
Logic current (DI=fixed, FCLK= 6MHZ)	Idd		1	1.4	mA
Input voltage (High)	VIH	0.7*VDD		VDD	V
Input voltage (Low)	VIL	0		0.3*VDD	V
Data input current (DI) High	I_{IH} DI			0.5	uA
Data input current (DI) Low	I_{IL} DI	-0.5			uA
STB (High)	I_{IH} STB			3	uA
STB (Low)	I_{IL} STB	-270			uA
Clock input current (High)	I_{IH} CLK			3	uA
Clock input current (Low)	I_{IL} CLK	-3			uA
Latch input current (High)	I_{IH} LAT			3	uA
Latch input current (Low)	I_{IL} LAT	-3			uA
Clock frequency	F_{CLK}			16	MHz
Clock width	T_W CLK	30			ns
Data setup time	T_{setup} DI	15			ns
Data hold time	T_{hold} DI	15			ns
Latch width	T_W LAT	40			ns
Latch Setup time	T_{setup} LAT	60			ns
Latch Hold time	T_{hold} LAT	30			ns
STB setup time	T_{setup} STB	300			ns
Driver out delay time	T_{do} (R_L=0.7KΩ, Vdd=24V, C_L=5pF)		4	8	us

Pad Coordinates

(The origin of the coordinates axes is the corner of the chip close to pad 156) unit : (um)

PAD Table (TBD)

Dimension and Package Information

Packaging: PAD locations of 128 bits chip driver as shown.

BUMP size：

1. X*Y=35um*60um for Don
2. X*Y=70um*35um for DIN, THPOUT, STB_B, STB_DIR, STB_OUT, VDD, VDD_OUT, DGND
3. X*Y=45um*35um for CLK, CLK_OUT, LAT_B, LAT_DIR, LAT_OUT

PAD pitch: X=58um between DOn
Chip thickness: 300um.
Chip size: 8440um*505um

PAD diagram （TBD）